Confirmation no.2298 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	GANGWAL, et al.	Examiner:	Treat, W.
Serial No.:	10/568,013	Group Art Unit:	2181
Filed:	February 10, 2006	Docket No.:	NL030979US1
Title:	PARALLEL PROCESSING ARRAY		

APPEAL BRIEF

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Dear Sir:

This Appeal Brief is submitted pursuant to 37 C.F.R. §41.37, in support of the Notice of Appeal filed October 27, 2008 and in response to the rejections of claims 1-32 and as set forth in the Final Office Action dated July 25, 2008.

Please charge Deposit Account number 50-0996 (NXPS.469PA) $540.00 for filing this brief in support of an appeal as set forth in 37 C.F.R. §1.17(c). If necessary, authority is given to charge/credit Deposit Account 50-0996 additional fees/overages in support of this filing.

I. Real Party In Interest

The real party in interest is NXP Semiconductors. The application is presently assigned of record, at reel/frame nos. 017598/0037 to Koninklijke Philips Electronics, N.V., headquartered in Eindhoven, the Netherlands. We have been authorized by both the assignee of record and NXP Semiconductors to convey herein that the entire right, title and interest of the instant patent application have been transferred to NXP Semiconductors.

II. Related Appeals and Interferences

While Appellant is aware of other pending applications owned by the above-identified Assignee, Appellant is unaware of any related appeals, interferences or judicial proceedings that would have a bearing on the Board's decision in the instant appeal.

III. Status of Claims

Claims 1-32 stand rejected and are presented for appeal. A complete listing of the claims under appeal is provided in an Appendix to this Brief.

IV. Status of Amendments

No amendments have been filed subsequent to the Office Action dated July 25, 2008.

V. Summary of Claimed Subject Matter

Appellant's recited invention relates to the use of a radio receiver that receives and processes data symbols transmitted along multiple paths. Each of the citations refers to the U.S.P.T.O. published version of Appellant's application.

Commensurate with independent claim 1, an example embodiment of the present invention is directed to a parallel processing array comprising a plurality of processing elements (PEs) (*e.g.*, FIG. 2, element 1; page 2, first column, lines 16-26), each processing element receiving a common instruction (*e.g.*, FIG. 2, element 10; page 2, first column, lines 33-59) and comprising: a multiplexer for receiving said common instruction (*e.g.*, FIG. 2, elements 5, 15 or 21; page 2, first column, lines 33-59); an arithmetic logic unit (*e.g.*, FIG. 2, element 3, page 2, first column, lines 20-26),

connected to said multiplexer, for processing the received instruction in association with an accumulator (*e.g.*, FIG. 2, element 3, page 2, first column, lines 20-26), and a flag register (*e.g.*, FIG. 2, element 9, page 2, first column, lines 20-26); characterized in that one or more of the processing elements in the processing array further comprises a storage element (*e.g.*, FIG. 2, element 11, page 2, first column, lines 28-59) having at least one storage location, the storage element configured to be indirectly addressable by the received instruction (*e.g.*, page 2, first column, lines 33-45), thereby enabling the processing of data dependent operations to be performed (*e.g.*, page 3, first column, lines 52-56).

Commensurate with independent claim 17, an example embodiment of the present invention is directed to a method of processing data in a parallel processing array comprising a plurality of processing elements (PEs) (*e.g.*, FIG. 2, element 1; page 2, first column, lines 16-26), each processing element receiving a common instruction (*e.g.*, FIG. 2, element 10; page 2, first column, lines 33-59) and comprising a multiplexer for receiving said common instruction (*e.g.*, FIG. 2, elements 5, 15 or 21; page 2, first column, lines 33-59), and an arithmetic logic unit (*e.g.*, FIG. 2, element 3, page 2, first column, lines 20-26), connected to said multiplexer, for processing the received instruction in association with an accumulator (*e.g.*, FIG. 2, element 3, page 2, first column, lines 20-26) and a flag register (*e.g.*, FIG. 2, element 9, page 2, lines 20-26), the method comprising the steps of: providing a storage element (*e.g.*, FIG. 2, element 11, page 2, first column, lines 28-59) in one or more of the processing elements in the processing array, the storage element having at least one storage location; configuring the storage element to be indirectly addressable by the received instruction (*e.g.*, page 2, first column, lines 33-45); and processing data dependent operations using the storage element (*e.g.*, page 3, first column, lines 52-56).

As required by 37 C.F.R. § 41.37(c)(1)(v), a concise explanation of the subject matter defined in the independent claims involved in the appeal is provided herein. Appellant notes that representative subject matter is identified for these claims; however, the abundance of supporting subject matter in the application prohibits identifying all textual and diagrammatic references to each claimed recitation. Appellant thus submits that other application subject matter, which supports the claims but is not specifically identified above, may be found elsewhere in the application. Appellant further notes that

this summary does not provide an exhaustive or exclusive view of the present subject matter, and Appellant refers to the appended claims and their legal equivalents for a complete statement of the invention.

VI. Grounds of Rejection to be Reviewed Upon Appeal

A. Claims 1-32 stand rejected under 35 U.S.C. § 112(1)

B. Claims 1-32 stand rejected under 35 U.S.C. § 112(2)

VII. Argument

As set forth below, Appellant submits that the claimed invention is allowable.

As background, Appellant's invention relates to parallel processing arrays, such as single instruction multiple data (SIMD) processing arrays. Such processing arrays contain a plurality of processing elements (PEs) that can each receive the same instruction, thereby performing the same operation in parallel. Such parallel processing arrays are well suited for performing highly repetitive tasks such as video processing (*see, e.g.*, Appellant's specification, published version, at paragraphs 0001-0003). Appellant realized that certain data dependent processing, such as retrieving data from a look-up table or performing different operations with different data elements of the same array, can exhibit poor efficiency in a SIMD processing array (*see, e.g.*, Appellant's specification paragraphs 006-007).

Appellant's claimed invention is generally directed toward circuitry/methodology for use with such parallel processing arrays. In particular, Appellant's claimed invention includes a local storage element in each PE. Aspects of Appellant's claimed invention are also directed to routing of data within the PE, such as routing data to and from the storage element. Aspects of Appellant's claimed invention include multiplexers that are used to route data within the PE. Appellant's specification teaches that a variety of different routing configurations are possible. The skilled artisan would recognize that reasonable variations from the expressly identified examples are readily possible. This disclosure relative to FIG. 2 of Appellant's specification is central to many of the issues in the present appeal. For the convenience of the Board, Appellant has reproduced FIG. 2 below. It should be apparent from a brief review of the figure that multiplexers 5, 15 and

21 allow for selective routing of data within the PE. It should also be apparent that instruction data (10) is taught to be received by each multiplexer at a control input to select the output of the multiplexers (*see also*, Appellant's specification at paragraph 0028). Each of these various routing possibilities is consistent with the general concept of providing/using an indirectly accessible memory within each PE (*see, e.g.*, Appellant's specification at paragraph 0045).

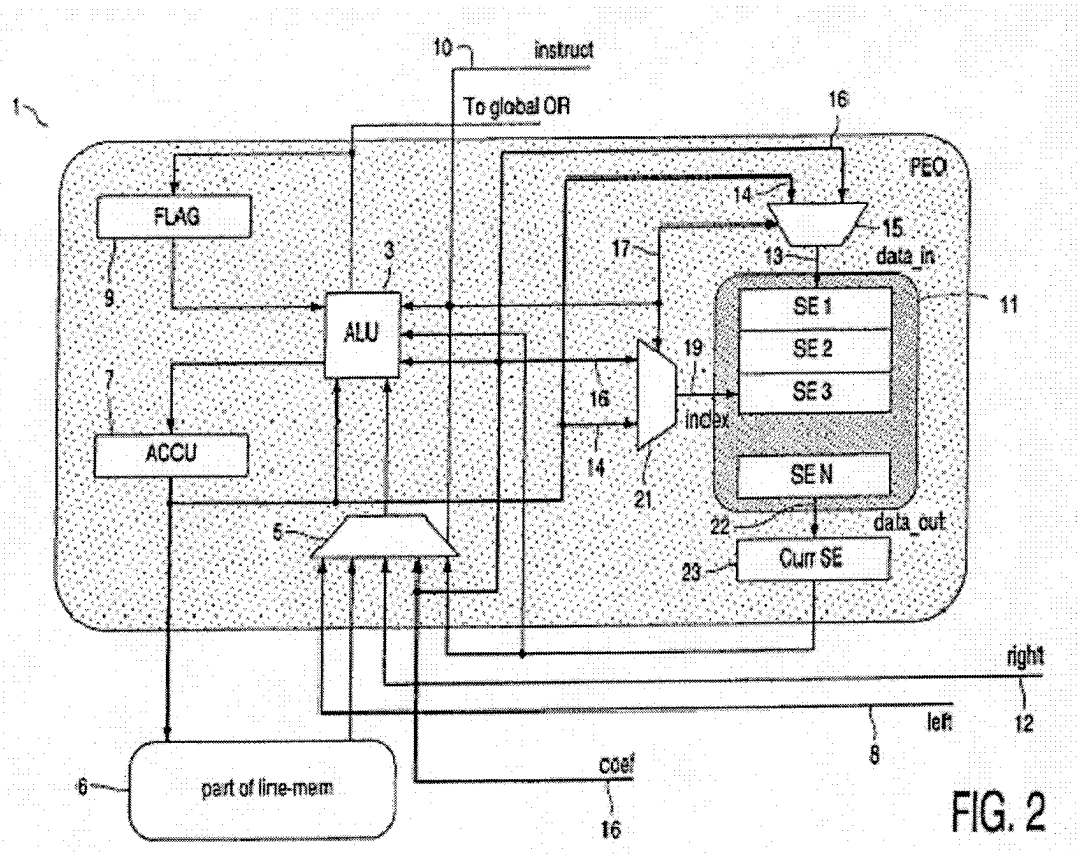

FIG. 2

It is important to note that the instant case being presented for appeal before the Examiner has applied all relevant statutory provisions of title 35 of the U.S. code. In pertinent part, MPEP § 2163 states:

> The above only describes how to determine whether the written description requirement of 35 U.S.C. 112, para. 1, is satisfied. Regardless of the outcome of that determination, Office personnel must complete the patentability determination under all the relevant statutory provisions of title 35 of the U.S. Code.
> Once Office personnel have concluded analysis of the claimed invention under all the statutory provisions, including 35 U.S.C. 101, 112, 102, and 103, they should review all the proposed rejections and their bases to confirm their correctness. Only then should any rejection be imposed in an Office action. The Office action should clearly communicate the findings, conclusions, and reasons which support them. When possible, the Office action should offer helpful suggestions on how to overcome rejections.

Despite this requirement, the Examiner has expressly refused to apply or analyze the claimed invention under all statutory provisions, choosing instead to only apply rejections under 35 U.S.C. § 112(2) and 35 U.S.C. § 112(1) (*see, e.g.*, Final Office Action of July 25, 2008 at page 4, paragraph No. 14). During prosecution Appellant has attempted to facilitate prosecution and work with the Examiner by making minor amendments to the figures and providing explanations for aspects that the Examiner expressed points of confusion. Appellant also requested that Examiner analyze the instant application under all relevant statutory provisions of title 35 of the U.S. Code (Final Office Action Response of September 5, 2008). The Examiner responded to Appellant's efforts by maintaining all rejections and refusing to apply or analyze claimed invention under all statutory provisions (see Advisory Action of September 15, 2008). The Examiner alleges that the requirement set forth in M.P.E.P. § 2163 does not apply. The Examiner does not support this allegation with a rule, law or court holdings. Appellant reiterates the request that the Examiner analyze the instant application under all relevant statutory provisions.

Regarding the rejections under 35 U.S.C. § 112(1), the deficiencies of the rejections are many and each of the deficiencies renders the rejections improper. For instance, MPEP 2164 states:

> when the subject matter is not in the specification portion of the application as filed but is in the claims, the limitation in and of itself may

> enable one skilled in the art to make and use the claim containing the limitation.

Therefore, a proper analysis under 35 U.S.C. § 112(1) should establish whether the experimentation needed to practice the invention is undue or unreasonable (M.P.E.P. § 2164.01 citing *Mineral Separation v. Hyde,* 242 U.S. 261, 270 (1916)). There are many factors to be considered when determining whether there is sufficient evidence to support a determination that a disclosure does not satisfy the enablement requirement and whether any necessary experimentation is "undue." The Examiner's analysis, however, begins and ends with an assertion that the figures and specification do not provide support for the limitations at issue. This assertion, however, is insufficient to establish a rejection under 35 U.S.C. § 112(1). A mere allegation that the specification does not provide express support is insufficient to support a conclusion of non-enablement. Moreover, the originally filed claims form part of the specification. Thus, the initial threshold for establishing a rejection under 35 U.S.C. § 112(1) has not been met.

When a proper analysis is undertaken for the limitations in question, it becomes apparent that the skilled artisan could readily implement the limitations without undue experimentation. This is true regardless of expressly identifying all limitations and embodiments in the description and figures. Each of the rejections relates to how data is routed to a multiplexer. Absent some reason that the skilled artisan would require undue experimentation to route data to multiplexers, after being shown the embodiments presented in and discussed in Appellant's specification, the rejections cannot stand. There is no such reason in the record because the limitations would not require undue experimentation. Further details of each specific limitation are discussed *infra.*

Regarding the rejections under 35 U.S.C. § 112(2), the rejections contain multiple deficiencies. For example, the rejections under 35 U.S.C. § 112(2) are deficient because they fail to identify which of the two separate requirements set forth in the second paragraph of 35 U.S.C. §112 apply. "If a rejection is based on 35 U.S.C. § 112, second paragraph, the examiner should further explain whether the rejection is based on indefiniteness or on the failure to claim what applicants regard as their invention. *Ex parte Ionescu*, 222 USPQ 537, 539 (Bd. App. 1984)." (M.P.E.P. § 2171). The Examiner

repeats both requirements in the rejection and provides a proper analysis for neither requirement.

The Examiner has not provided an analysis of the rejections in view of either of the requirements. This confusion is perhaps related to the Examiner's improper attempts to use analyses under 35 U.S.C. § 112(1) to support the rejections under 35 U.S.C. § 112(2) (*see, e.g.*, Final Office Action of July 25, 2008, where the entirety of the analysis simply refers to an analysis presented to support a rejection under 35 U.S.C. § 112(1)). The only evidence of the record is an allegation that one or more specific limitations are not expressly found in the figures and/or detailed description. The absence of express support for particular limitations does not prove that either of the two requirements has not been met. For instance, the skilled artisan is not shown to require undue experimentation simply because a limitation is not expressly shown in a figure. Therefore, the record shows that Examiner has not properly considered the factors for either of the requirements for a 35 U.S.C. § 112(2) rejection.

The following arguments further detail the impropriety of the rejections. Each heading and subheading represents a distinct grouping of claims for which the arguments that follow apply. Accordingly, the claims do not stand and fall together for each and every argument and should be grouped consistent with the headings.

Appellant therefore requests that the Board reverse the rejections for the reasons put forth herein.

A. The § 112(1) Rejection Of Claims 1-32 Is Improper And Should Be Reversed Because The Examiner Has Not Considered The Disclosure Of The Originally Filed Claims.

The Examiner has not presented a *prima facie* case for a 35 U.S.C. § 112(1) rejection. The full extent of support for the rejection is an erroneous allegation by the Examiner that FIG. 2 and Appellant's specification do not explicitly support one of two different aspects (*i.e.*, a multiplexer for receiving a common instruction and an index multiplexer for passing the received instruction). This level of analysis, however, is insufficient. For instance, the analysis fails to acknowledge and address that these aspects were part of the original claims. The record is clear that each of the claim limitations in question was present when the application was filed. The Examiner has not

provided any explanation as to the level of the skilled artisan. This explanation would be necessary for any analysis as to why the skilled artisan would not find the originally-filed claims enabled. The rejections, therefore, fail because there is no evidence, explanation or analysis that supports that the skilled artisan would require undue experimentation to implement the aspects at issue.

The substance of each of the rejections relates to various ways of routing of data within a PE. There is no evidence presented as to why the skilled artisan would need to resort to undue experimentation to implement these ways of routing data. At best, the Examiner has merely asserted that the claim limitations are not explicitly described in the specification and the figures. Moreover, Appellant's disclosure teaches a variety of different data-routing options, thereby teaching the skilled artisan how to implement routing of several different types of data. In view of these teachings, the relatively mature nature of the technology, and the level of skill of the person of ordinary skill in the art, the skilled artisan would be able to implement reasonable variations from the expressly taught embodiments. These reasonable variations would include different data routing to the multiplexers.

Accordingly, each of the 35 U.S.C. § 112(1) rejections is improper and should be reversed. Moreover, as will be discussed in more detail below, the record establishes that various aspects are fully supported by the figures and detailed description of Appellant's Application. Accordingly, the rejections under 35 U.S.C. § 112(1) should be reversed, generally, for the aforementioned reasons, and more specifically for the individually based reasons hereafter. Each of these reasons is sufficient to render the rejections improper and reversible.

1. The § 112(1) rejection of claims 1 and 17 and (through dependency) claims 2-16 and 18-32, is improper and should be reversed because there is no dispute that the limitations are fully supported and Appellant has not been afforded the benefit of disclosures of the originally filed claims.

The basis for one of the rejections under 35 U.S.C. § 112(1) stems from limitations of independent claims 1 and 17. This rejection is improper as the specification supports the limitations at issue. Although the Examiner has maintained the

rejection, the Examiner has agreed that the limitations are supported. The Examiner agrees that instruction data is sent to control the multiplexer. Data that is sent to a multiplexer for the purpose of controlling the multiplexer is received by that multiplexer, and therefore, the only remaining issue is with regards to dependent claims 4 and 20 (see Advisory Action of September 15, 2008). Appellant addresses the rejection of claims 4 and 20 in the next section (2) of the argument. As there is no remaining issue of fact for claims 1 and 17, the rejection should have been removed. Notwithstanding, the following discussion provides further evidence of enablement.

The Examiner mistakenly asserts that there is no support for limitations directed to a multiplexer for receiving a common instruction (*see, e.g.*, Final Office Action of July 25, 2008 at page 3, bullet point 6). In the same paragraph, the Examiner acknowledges that all of the multiplexers are controlled by the instruction data. As taught by Appellant's specification (*see, e.g.*, FIG. 2, showing instruction 10 being received by multiplexers 5, 15 and 21) the instruction data arrives at (and is therefore received by) various multiplexers to allow control thereof. These teachings of Appellant's specification, collaborated by the Examiner's independent conclusions thereof, provide explicit support for the limitations directed to receiving instruction data at the multiplexer. Under the plain meaning of the term receiving, along with the description found in Appellant's specification, the limitations at issue are fully supported (*i.e.*, receiving instruction data at a control input of a multiplexer is receiving instruction data at the multiplexer). The Examiner has independently interpreted Appellant's specification to teach that instruction data arrives at (and is therefore received by) each of the multiplexers. Accordingly, the record shows that Appellant's specification teaches that instruction data is received at the multiplexers.

Moreover, the limitations at issue were part of the originally filed application. A proper analysis for an enablement rejection would therefore require analysis and explanation regarding the level of skill for a hypothetical skilled artisan in the technology. This analysis should further explain why this skilled artisan would need to resort to undue experimentation to implement the invention. Given the mature nature of the parallel processor array technology, the general concepts of a storage element in each PE and multiplexers to selectively route data within the PE, and Appellant's originally

filed claims, the skilled artisan would be able to implement a PE that received instruction data at a multiplexer.

Accordingly, the Section 112(1) rejection of claims 1-32, based upon limitations of claims 1 and 17, must be reversed.

2. The § 112(1) rejection of claims 4 and 20 is improper because the disclosure present in the originally-filed claims should have been considered, and therefore, the skilled artisan would have been able to implement the claim limitations without undue experimentation.

The record is clear that the claim limitations at issue (*i.e.*, an index multiplexer to pass received instruction data) were present at the time of filing. The only argument put forth in support of the rejection is an assertion that Appellant's figures and specification do not support the claim limitations at issue. This, however, is at least partially incorrect because Appellant's specification includes the claims. The Examiner's analysis is simply an assertion that Appellant's figures and detailed description do not explicitly disclosure certain aspects. The Examiner summarily concludes that this assertion is sufficient for the rejection; however, there is no articulated rationale to support a rejection of non-enablement. Particularly, there is neither evidence nor analysis to support a finding that the skilled artisan would need to resort to undue experimentation to route instruction data so that it could be passed by the index multiplexer of FIG. 2. The analysis should consider that the skilled artisan would have the benefit of first reading Appellant's disclosure, which explains the basic configurations of the index multiplexer and a few example types of data that can be passed by the multiplexer. After being presented with the idea to do so (as found in the originally filed claims 4 and 20), the skilled artisan would readily be able to route data to the index multiplexer. Accordingly, claims 4 and 20 sufficiently define the functionality of the multiplexer such that the skilled artisan would be able to create a circuit by a reasonable modification of FIG. 2 to include an index multiplexer that also passed instruction data.

For at least the aforementioned reasons, the 35 U.S.C. § 112(1) rejection of claims 4 and 20 must be reversed.

B. The § 112(2) Rejection of Claims 1-32 is Improper and Should Be Reversed Because A Proper Basis For The Rejections Has Not Been Presented.

1. The § 112(2) rejection of claims 1 and 17 and (through dependency) claims 2-16 and 18-32, is improper and should be reversed because the Examiner improperly analyzes the rejections under the framework of a § 112(1) rejection.

The rejection under 35 U.S.C. § 112(2) for limitations found in claims 1 and 17 is improper because the record does not establish a proper basis for a 35 U.S.C. § 112(2) rejection. There are two different requirements of 35 U.S.C. § 112(2) rejections, each of which requires different analysis and evidence to establish a proper rejection. M.P.E.P. § 2171 explains that:

> (A) the claims must set forth the subject matter that applicants regard as their invention; and
>
> (B) the claims must particularly point out and distinctly define the metes and bounds of the subject matter that will be protected by the patent grant.

The Examiner has not identified which requirement is lacking and has not presented an argument for either requirement. The first limitation requires a statement by the Appellant, other than the specification, that indicates that the invention is other than that which is claimed (see M.P.E.P. § 2172). There are no such statements in the record. The primary purpose of the second requirement is to ensure that the scope of the claims is clear so the public is informed of the boundaries of what constitutes infringement of the patent (see M.P.E.P. § 2173). The Examiner's rejection evidences that the Examiner had no trouble understanding the claim limitations. For instance, the Examiner provides clear and definite interpretations of the claim limitations (see Final Office Action of July, 25, 2008 at page 3). The Examiner then merely alleges that these clear and definite interpretations are not found in Appellant's disclosure (see Final Office Action of July, 25, 2008 at pages 3 and 4). Allegations of lack of support in the disclosure do not establish that a rejection under 35 U.S.C. § 112(2) is proper.

Notwithstanding the deficiencies in the support for the rejection, the claims particularly point out and distinctly claim the subject matter which the Appellant regards

as his invention. The claim limitations at issue contain relatively straight-forward language that is directed to instruction data being received by a multiplexer. The skilled artisan would recognize that Appellant regarded these limitations are part of the claimed invention because these limitations were present in the originally-filed claims. Moreover the scope of the limitations is clear and distinct (*i.e.*, whether or not instruction data is received by the multiplexer). This is further supported by the Examiner's ability to understand the scope of the limitations and thereby (improperly) assert that the limitations are shown in the figures.

Accordingly, the 35 U.S.C. § 112(2) rejection of claims 1-32, based upon limitations of claims 1 and 17, must be reversed.

2. The § 112(2) rejection of claims 4 and 20 is improper and should be reversed because the Examiner does not allege any deficiencies in the claims that would be relevant to a § 112(2) rejection.

The rejection under 35 U.S.C. § 112(2) for limitations found in claims 4 and 20 is improper because the record does not establish a proper basis for a 35 U.S.C. § 112(2) rejection. There are two different requirements of 35 U.S.C. § 112(2) rejections, each of which requires different analysis and evidence to establish a proper rejection. M.P.E.P. § 2171 explains that:

> (A) the claims must set forth the subject matter that applicants regard as their invention; and
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The Examiner has not identified which requirement is lacking and has not presented an argument for either requirement. The first limitation requires a statement by the Appellant, other than the specification, that indicates that the invention is other than that which is claimed (see M.P.E.P. § 2172). There are no such statements in the record. The primary purpose of the second requirement is to ensure that the scope of the claims is clear so the public is informed of the boundaries of what constitutes infringement of the patent (see M.P.E.P. § 2173). The Examiner's rejection evidences that the Examiner had no trouble understanding the claim limitations. For instance, the Examiner provides clear

and definite interpretations of the claim limitations (see Final Office Action of July, 25, 2008 at page 3). The Examiner then merely alleges that these clear and definite interpretations are not found in Appellant's disclosure (see Final Office Action of July, 25, 2008 at pages 3 and 4). Allegations of lack of support in the disclosure do not establish that a 35 U.S.C. § 112(2) is proper.

The claims particularly point out and distinctly claim the subject matter which the applicant regards as his invention. The skilled artisan would recognize that Appellant regarded these limitations are part of the claimed invention because these limitations were present in the originally-filed claims. The claim limitations at issue contain relatively straight-forward language that is directed to instruction data being passed by a multiplexer. The scope is clear and distinct (*i.e.*, whether or not instruction data is passed by the multiplexer), which is further supported by the Examiner's independent ability to ascertain the scope of the claims in discussion of the various rejections.

Accordingly, the 35 U.S.C. § 112(2) rejection of claims 4 and 20 must be reversed.

3. The § 112(2) rejection of claims 7 and 23 is improper and should be reversed because the accumulator data is used as coefficient data.

The rejections of claim 7 and 23 for lack of written description are improper because the Examiner has not presented a case that the claims fail to point out and distinctly claim the invention and because the Examiner has improperly interpreted Appellant's claims and/or specification.

The Examiner's rejection asserts that essential elements were omitted; however, the relied upon section of the M.P.E.P., § 2172.01, does not support a rejection under 35 U.S.C. §112(2) for such an omission. In pertinent part, M.P.E.P. § 2172.01 states that:

> A claim which omits matter disclosed to be essential to the invention as described in the specification or in other statements of record may be rejected under 35 U.S.C. 112, first paragraph, as not enabling.

It would, therefore, appear that the Examiner is improperly applying the standards from 35 U.S.C. § 112(1) to a 35 U.S.C. § 112(2) rejection. The analysis of a

35 U.S.C. § 112(1) rejection is different from that of a 35 U.S.C. § 112(2) and misapplying a standard from one type of rejection to another is not sufficient to support a rejection of either type. Accordingly, the rejection is improper due to the Examiner's failure to perform the proper analysis for a rejection under either 35 U.S.C. § 112(1) or under 35 U.S.C. § 112 (2).

Notwithstanding, the record shows that the claims do not omit an essential step. The Examiner's rejection incorrectly assumes that an essential "transformation" step is missing because claims 7 and 23 relate to passing accumulator data through a multiplexer and at the same time storing coefficient data in the storage element linked to the multiplexer. Appellant previously explained (see Final Office Action Response of April 30, 2008) that there is no missing transformation step. Simply put, data of a first (accumulator) type is passed through the multiplexer and then stored and used as a second (coefficient) type. The Examiner chose not to respond to Appellant's argument, which is presented hereafter in more detail.

The storage element can be used to facilitate operations where PEs each use different coefficients based on location of data in an array (*see, e.g.*, Appellant's specification at paragraph 0044). Thus, the data in the storage element (11) is coefficient data regardless of the original source of the data. The input to the storage element can be either coefficient data (16) or accumulator data (14) and is controlled by multiplexer 15 (*see, e.g.*, FIG. 2, (15) and Appellant's specification at paragraph 0032). Thus, when the multiplexer 15 is passing accumulator data, the storage element is storing the data for use as coefficient data. Accordingly, there is no missing "transformation" step because the accumulator data passed by multiplexer 15 becomes coefficient data once stored in the storage element.

Accordingly, the 35 U.S.C. § 112(2) rejection of claims 7 and 23 must be reversed.

VIII. Conclusion

In view of the above, Appellant submits that the rejections of claims 1-32 are improper. Appellant therefore requests reversal of the rejections as applied to the appealed claims and allowance of the entire application.

Authority to charge the undersigned's deposit account was provided on the first page of this brief.

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APPENDIX OF CLAIMS INVOLVED IN THE APPEAL
(S/N 10/568,013)

1. A parallel processing array comprising a plurality of processing elements (PEs), each processing element receiving a common instruction and comprising: a multiplexer for receiving said common instruction; an arithmetic logic unit, connected to said multiplexer, for processing the received instruction in association with an accumulator and a flag register; characterized in that one or more of the processing elements in the processing array further comprises a storage element having at least one storage location, the storage element configured to be indirectly addressable by the received instruction, thereby enabling the processing of data dependent operations to be performed.

2. A parallel processing array as claimed in claim 1, wherein the storage element comprises: an input data port for receiving data to be stored; an index signal for addressing a storage location in the storage element; and an output port for outputting data from the storage element.

3. A parallel processing array as claimed in claim 2, wherein the input data port of the storage element is connected to receive data from an input multiplexer, the input multiplexer being configured to pass accumulator data or coefficient data.

4. A parallel processing array as claimed in claim 2, wherein the index signal is received from an index multiplexer, the index multiplexer being configured to selectively pass accumulator data or coefficient data, or part of the received instruction.

5. A parallel processor as claimed in claim 3, wherein the input multiplexer and/or index multiplexer is controlled by the received instruction.

6. A parallel processing array as claimed in claim 1, wherein the storage element is configured to provide the processing element with a coefficient based on the data to be processed.

7. A parallel processing array as claimed in claim 6, wherein the input multiplexer is configured to pass accumulator data to the storage element when coefficient data is being stored in a storage location defined by the index signal.

8. A parallel processing array as claimed in claim 6, wherein the input multiplexer is configured to pass coefficient data to the storage element, stored in a storage location defined by the index signal.

9. A parallel processing array as claimed in claim 7, wherein the index signal is defined by coefficient data received by the index multiplexer.

10. A parallel processing array as claimed in claim 7, wherein the index signal is defined by accumulator data received by the index multiplexer.

11. A parallel processing array as claimed in claim 1, wherein the storage element is configured to provide a local look-up table for the processing element.

12. A parallel processing array as claimed in claim 11, wherein the input multiplexer is configured to pass coefficient data to the storage element for storage in a location defined by the index signal.

13. A parallel processing array as claimed in claim 12, wherein the index signal is defined by accumulator data received by the index multiplexer.

14. A parallel processing array as claimed in claim 11, wherein the input multiplexer is configured to pass a first part of the coefficient data as the data to be stored in the storage element, and the index multiplexer arranged to pass the other part of the coefficient data as the index signal defining the storage address.

15. A parallel processing array as claimed in claim 1, further comprising a register for storing data between the output of the storage element and the input of the multiplexer.

16. A parallel processing array as claimed in claim 1, wherein the processing array is a single instruction multiple data (SIMD) processing array.

17. A method of processing data in a parallel processing array comprising a plurality of processing elements (PEs), each processing element receiving a common instruction and comprising a multiplexer for receiving said common instruction, and an arithmetic logic unit, connected to said multiplexer, for processing the received instruction in association with an accumulator and a flag register, the method comprising the steps of: providing a storage element in one or more of the processing elements in the processing array, the storage element having at least one storage location; configuring the storage element to be indirectly addressable by the received instruction; and processing data dependent operations using the storage element.

18. A method as claimed in claim 17, further comprising the steps of: providing an input data port in the storage element for receiving data to be stored; providing an index signal for addressing a storage location in the storage element; and providing an output port for outputting data from the storage element.

19. A method as claimed in claim 18, further comprising the steps of connecting the input data port of the storage element to receive data from an input multiplexer, and configuring the input multiplexer to pass accumulator data or coefficient data.

20. A method as claimed in claim 18, further comprising the step of providing an index multiplexer for providing the index signal, and configuring the index multiplexer to selectively pass accumulator data or coefficient data, or part of the received instruction.

21. A method as claimed in claim 19, further comprising the step of controlling the input multiplexer and/or index multiplexer with the received instruction.

22. A method as claimed in claim 17, further comprising the step of configuring the storage element to provide the processing element with a coefficient based on the data to be processed.

23. A method as claimed in claim 22, further comprising the step of configuring the input multiplexer to pass accumulator data to the storage element when coefficient data is being stored in a storage location defined by the index signal.

24. A method as claimed in claim 22, further comprising the step of configuring the input multiplexer to pass coefficient data to the storage element, and storing the coefficient data in a storage location defined by the index signal.

25. A method as claimed in claim 23, wherein the index signal is defined by coefficient data received by the index multiplexer.

26. A method as claimed in claim 23, wherein the index signal is defined by accumulator data received by the index multiplexer.

27. A method as claimed in claim 17, further comprising the step of configuring the storage element to provide a local look-up table for the processing element.

28. A method as claimed in claim 27, wherein the input multiplexer is configured to pass coefficient data to the storage element for storage in a location defined by the index signal.

29. A method as claimed in claim 28, wherein the index signal is defined by accumulator data received by the index multiplexer.

30. A method as claimed in claim 27, further comprising the step of configuring the input multiplexer to pass a first part of the coefficient data as the data to be stored in the storage element, and arranging the index multiplexer to pass the other part of the coefficient data as the index signal defining the storage address.

31. A method as claimed in claim 17, further comprising the step of providing a register for storing data between the output of the storage element and the input of the

multiplexer.

32. A method as claimed in claim 17, wherein the processing array is a single instruction multiple data (SIMD) processing array.

APPENDIX OF EVIDENCE

Appellant is unaware of any evidence submitted in this application pursuant to 37 C.F.R. §§ 1.130, 1.131, and 1.132.

APPENDIX OF RELATED PROCEEDINGS

As stated in Section II above, Appellant is unaware of any related appeals, interferences or judicial proceedings.